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Design for Testability Strategies for System-on-Chip and System-in-Package Technologies

Presenter

Prof. Andrew Richardson
Centre for Microsystems Engineering
Lancaster University

Date & Venue

3 Days 4th—6th December 2006
ISLI, Livingston

Cost

£950 per person + VAT

10% discount for 6 or more
20% discount for 10 or more
(from same company site)

Contact

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Course Aims

To provide delegates with an understanding of test issues and solutions for SoC and SiP technologies and provide delegates with the ability to optimise the testability of products based on both these integration solutions. Embedded test functions and Built-in Test Strategies (BIST) will be covered in detail.

The course is organised into four themes: An introduction to SoC and SiP technology, Test and measurement basics, SoC and SiP test strategies and embedded test solutions for core functions.

Target Audience

Industrial design engineers responsible for designing testability into core functions or Integration platforms, test engineers responsible for design and implementation of production test solutions, academics and postgraduate students with interests in system test. The 1st day will provide all necessary analogue background in both SoC and SiP technology and their interfaces

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Course Content

Status & Future Requirements for Analog Test

- International technology and test trends
- Innovation and future demands for analogue test engineering
- Test cost
- Quality and time to market requirements
- Analogue test bottlenecks
- Design and test flow

Basic Analog Test Techniques

- Analogue specifications and measurement techniques (for typical analogue functions)
- Stimulus generation
- Engineering test strategies
- Instrumentation
- Core bench skills

Analog Design & Test Integration

- State-of-the-art in analogue DfT
- Test access methods
- Built-in test
- Self-test
- Online monitoring

Analog Test Support

- Fault and defect modelling
- Fault extraction
- Fault simulation techniques and sensitivity analysis
- Pattern generation
- Virtual test and test quality metrics

Presenter

The Centre for Microsystems Engineering specialises in industrially linked projects in the field of mixed signal design and test technology for both SoC and microsystem (smart sensor) applications.

The scope of work extends from device and defect physics to test issues related to design reuse and computer aided design and test tools.

Fees

Fees cover tuition, course notes, lunches and light refreshments.

Registration & Enquiries

Please contact Tracy Whitefield for further information on any aspects of the training course or to make a provisional booking.

Accommodation

Information on local hotels is available at www.sli-institute.ac.uk/facilities/smcc.htm.
http://www.frontdesk.co.uk/isli

Cancellations

A 10% administration fee is levied for cancellations made up to two weeks prior to the start of the course. Cancellations thereafter will be liable to the loss of the full fee. Substitutions may be made at any time up till the start of the course.

The Institute reserves the right to cancel an advertised course at short notice or to postpone or make such alterations to the content of a course as may be necessary.

If a course is cancelled, fees will be refunded in full.

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